

FIG. 1B

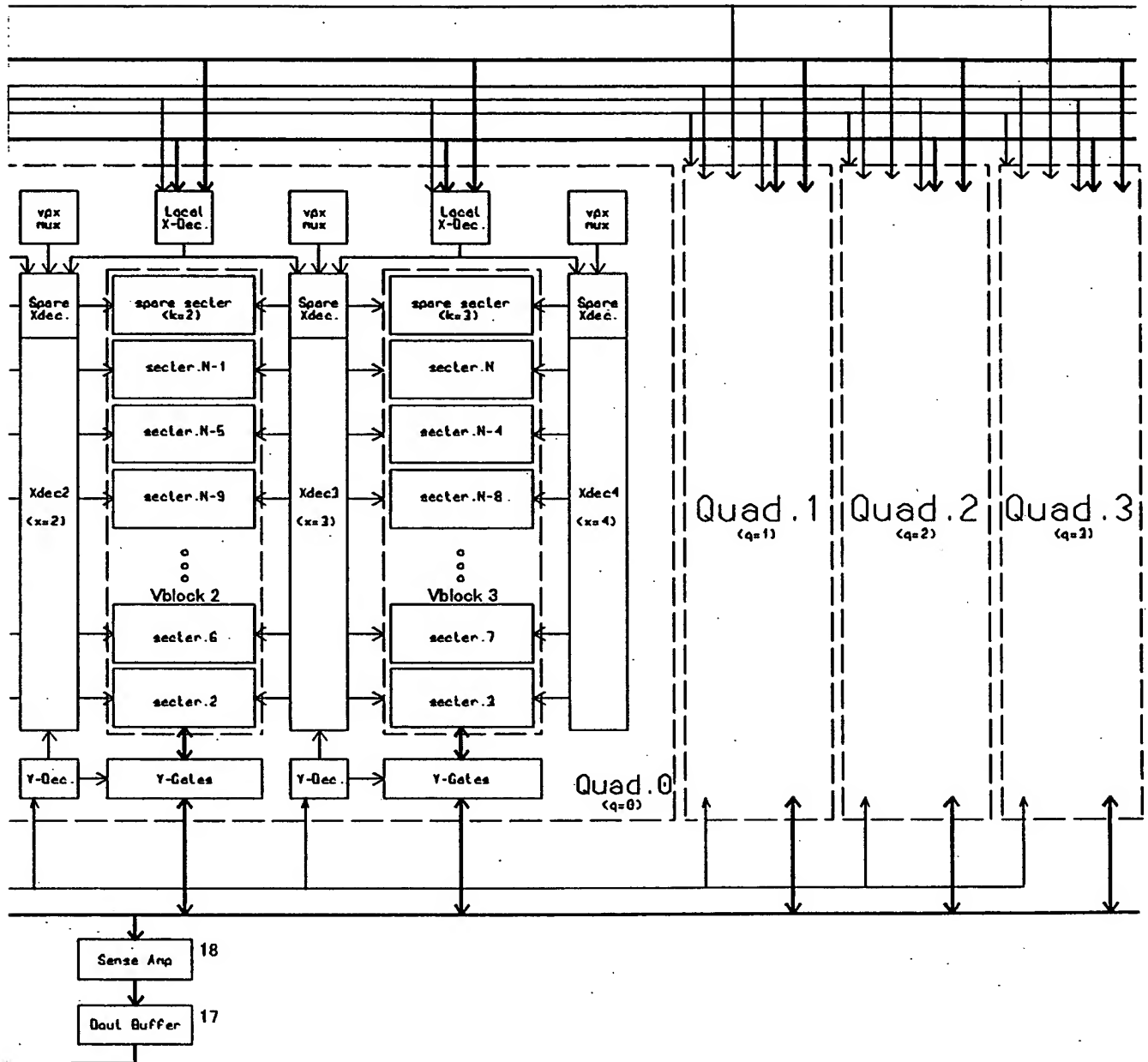
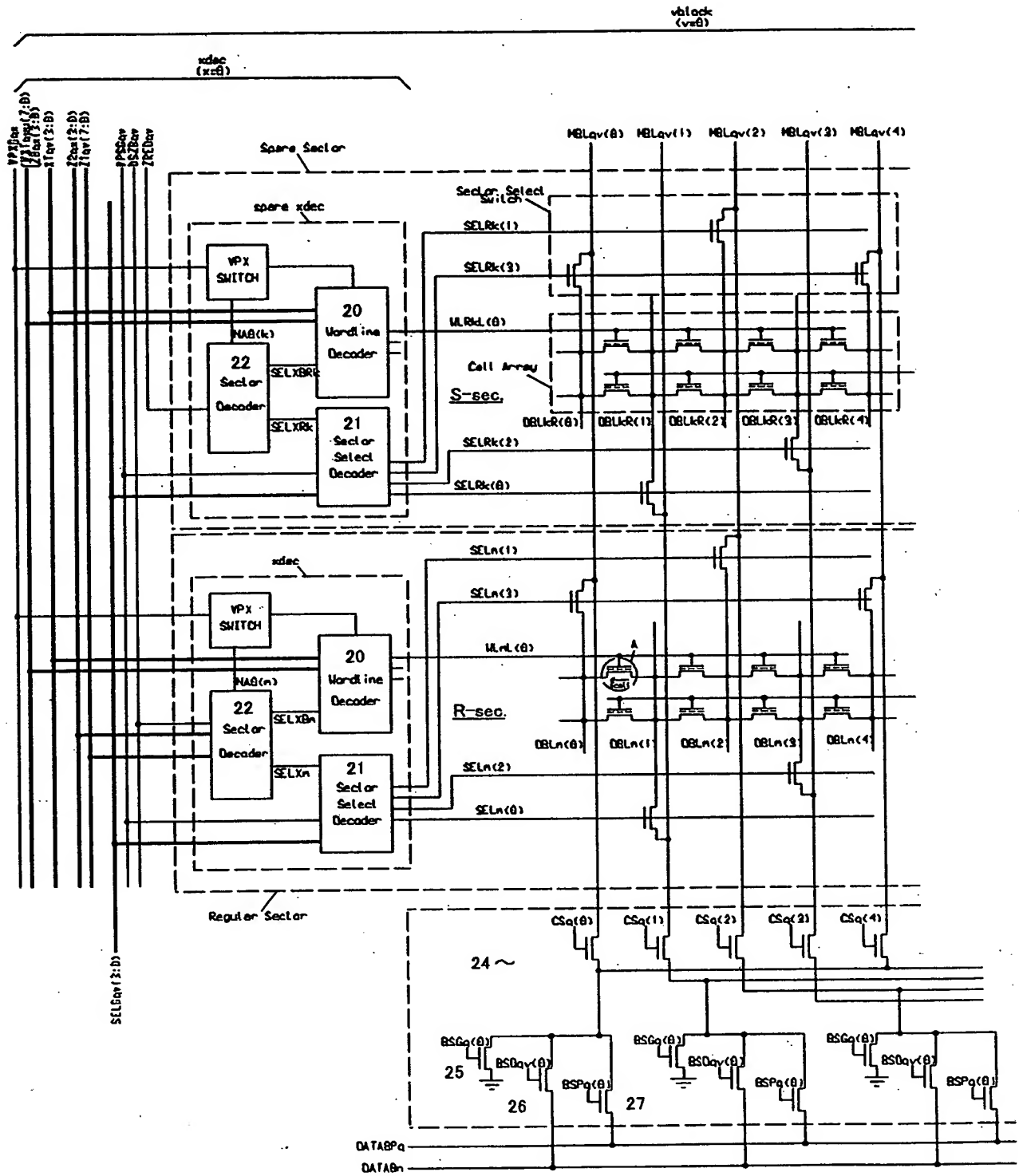


FIG. 2A



**FIG. 2B**

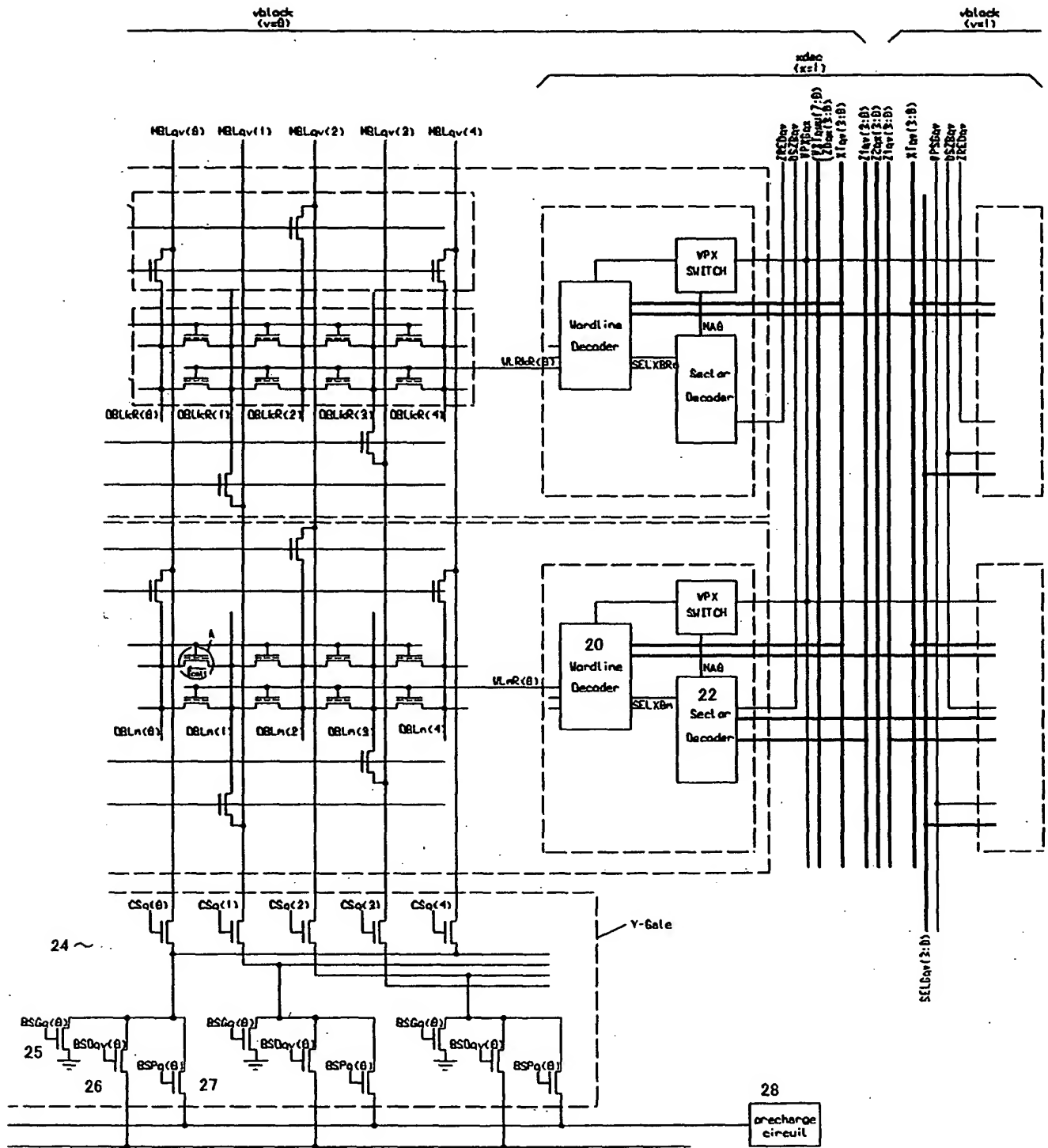


FIG. 3

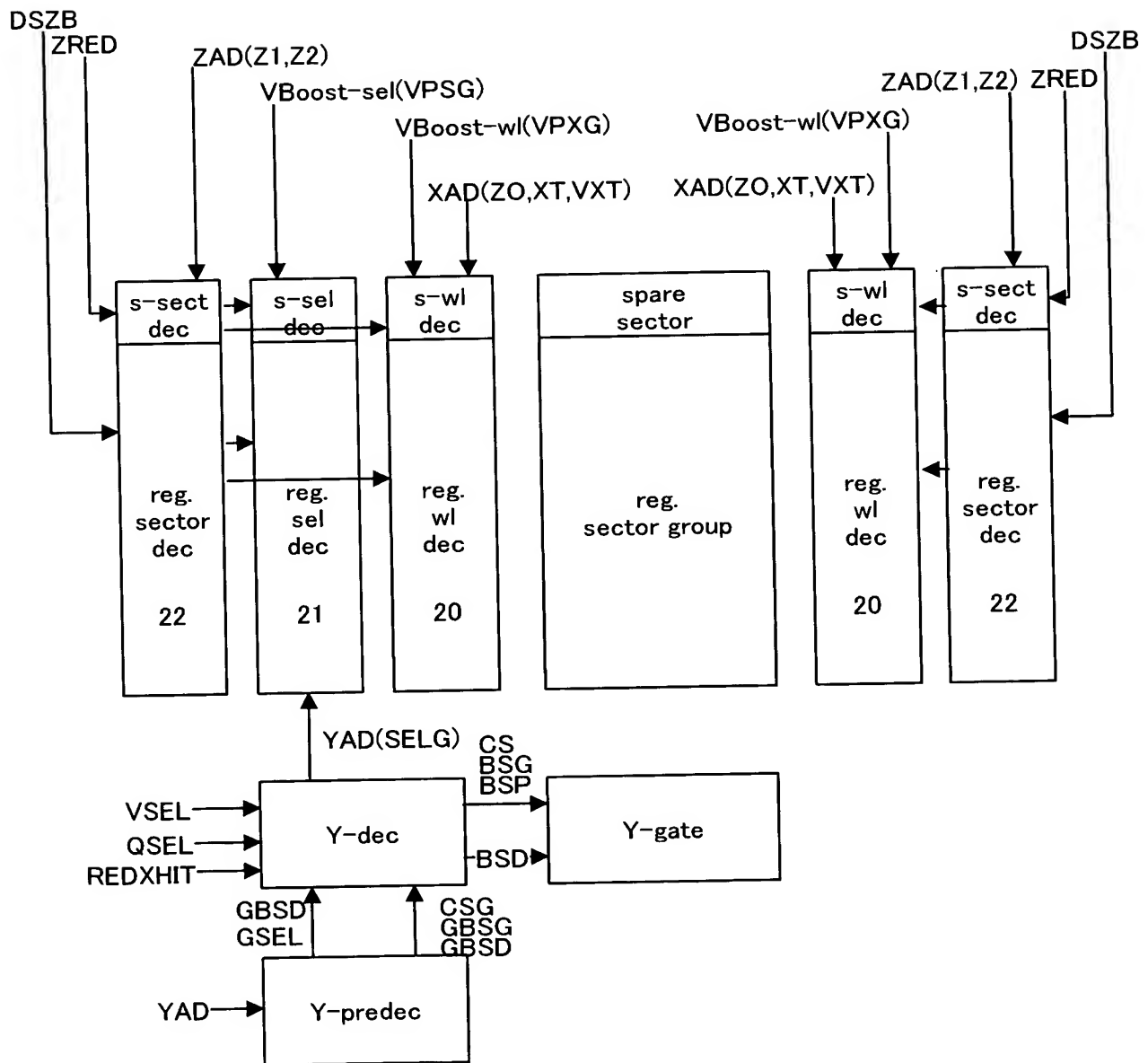


FIG. 4

Simultaneously Selected State for Regi WL and Spare WL

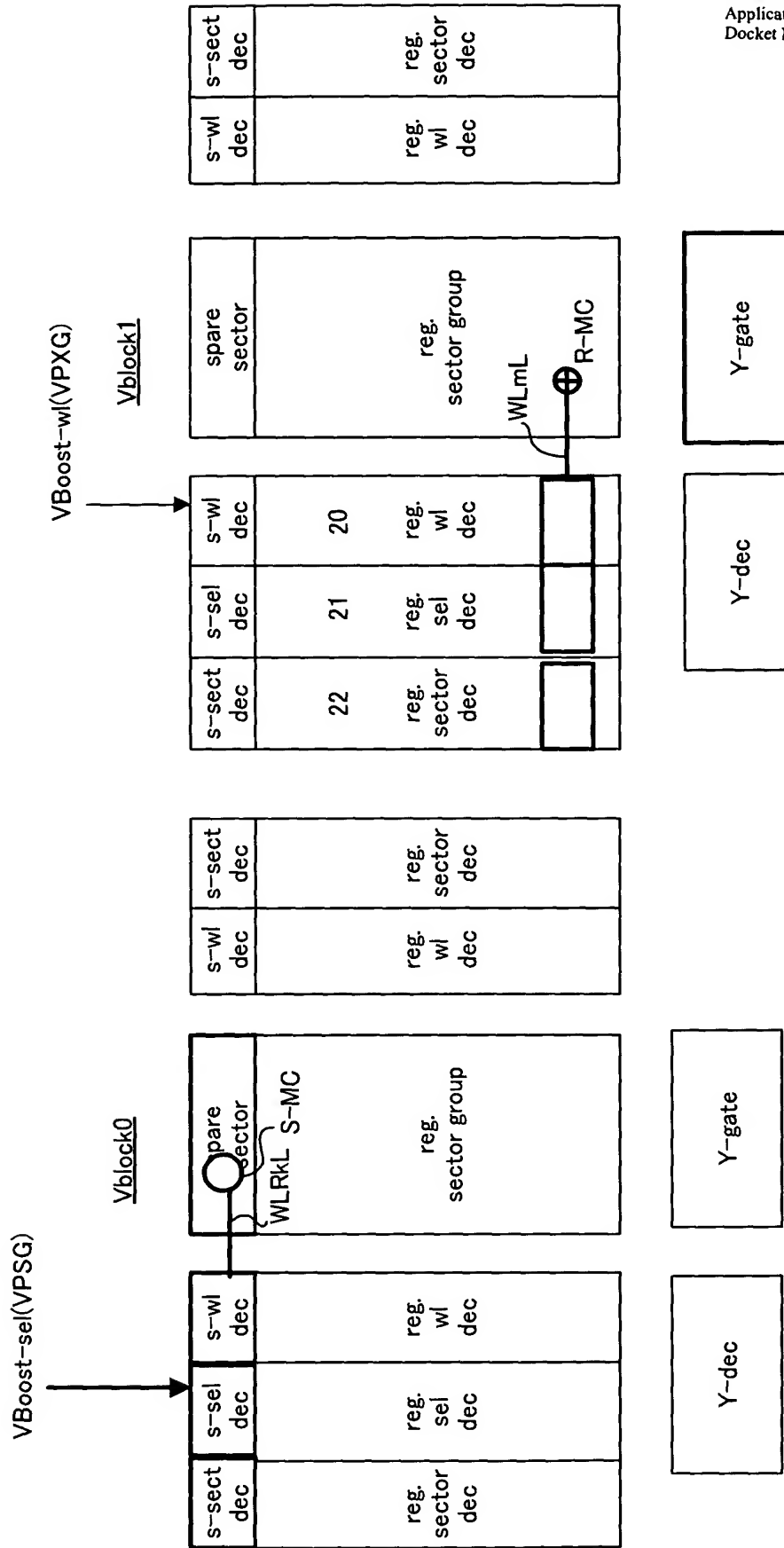


FIG. 5

Redundancy Address is Matched

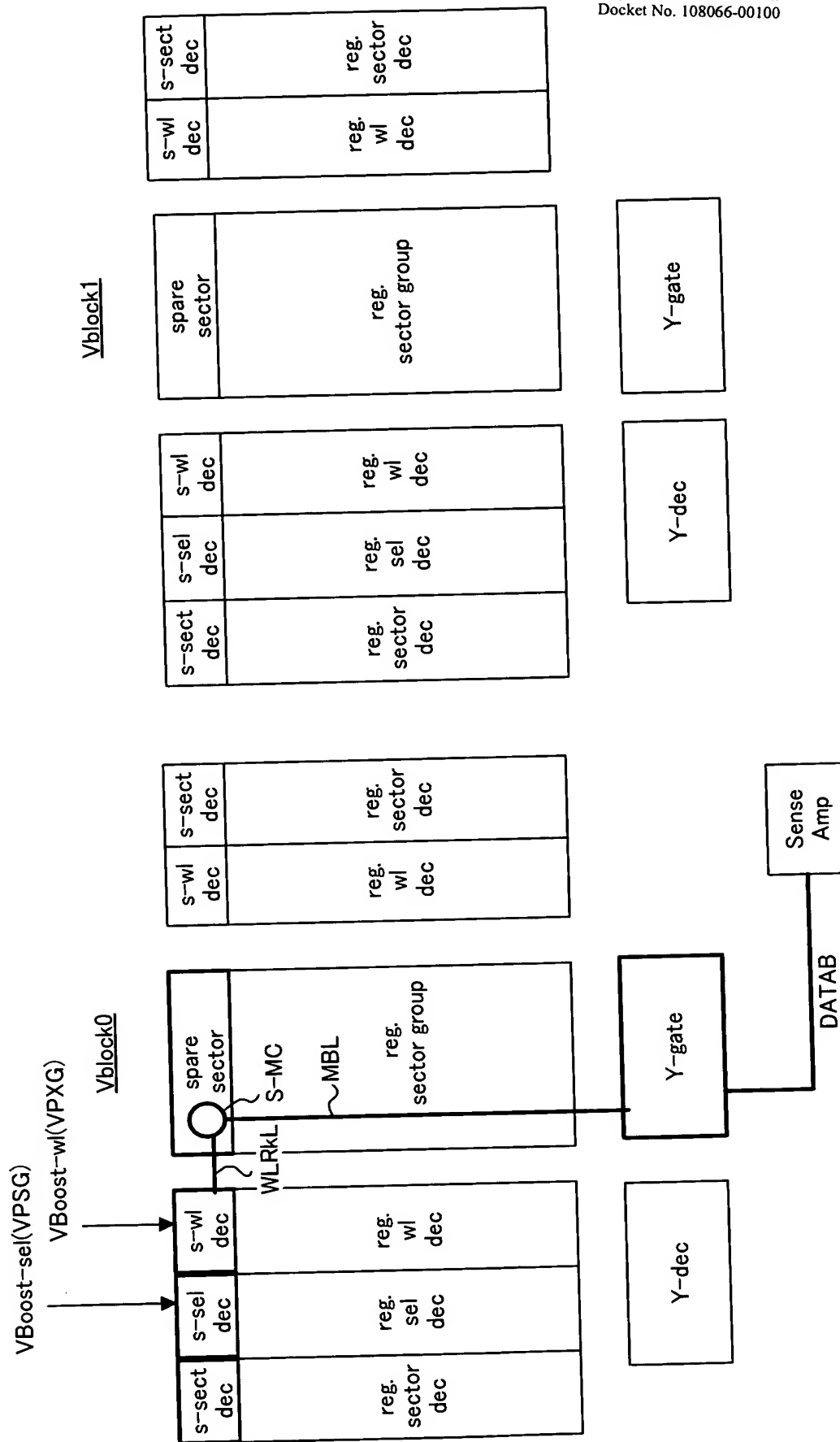
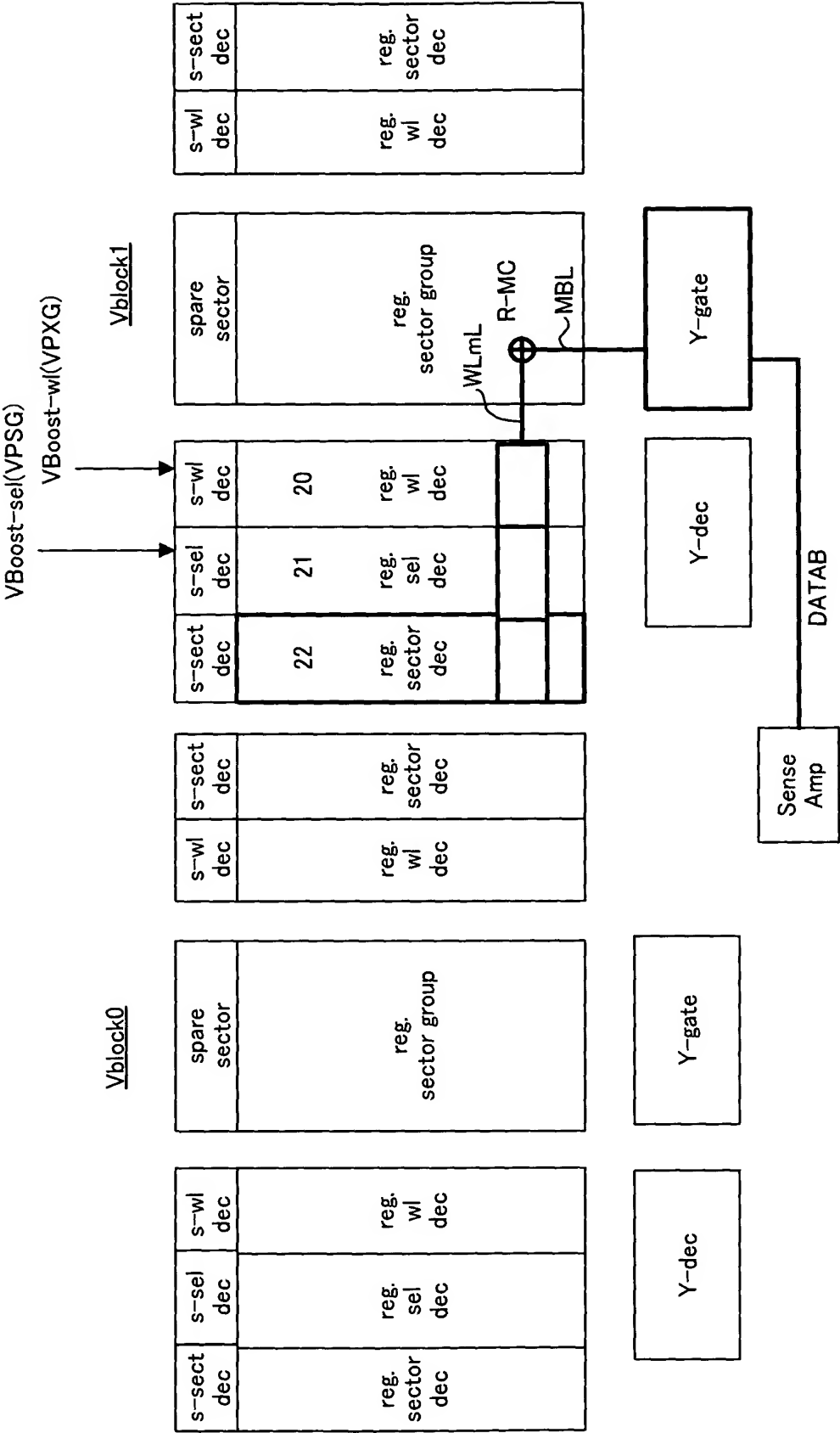


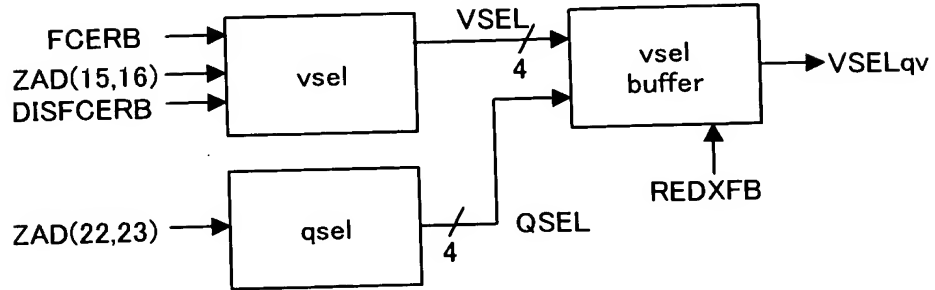
FIG. 6

Redundancy Address is Mismatched





**FIG. 7** Vertical Block Select Signal Buffer Circuit



**FIG. 8**

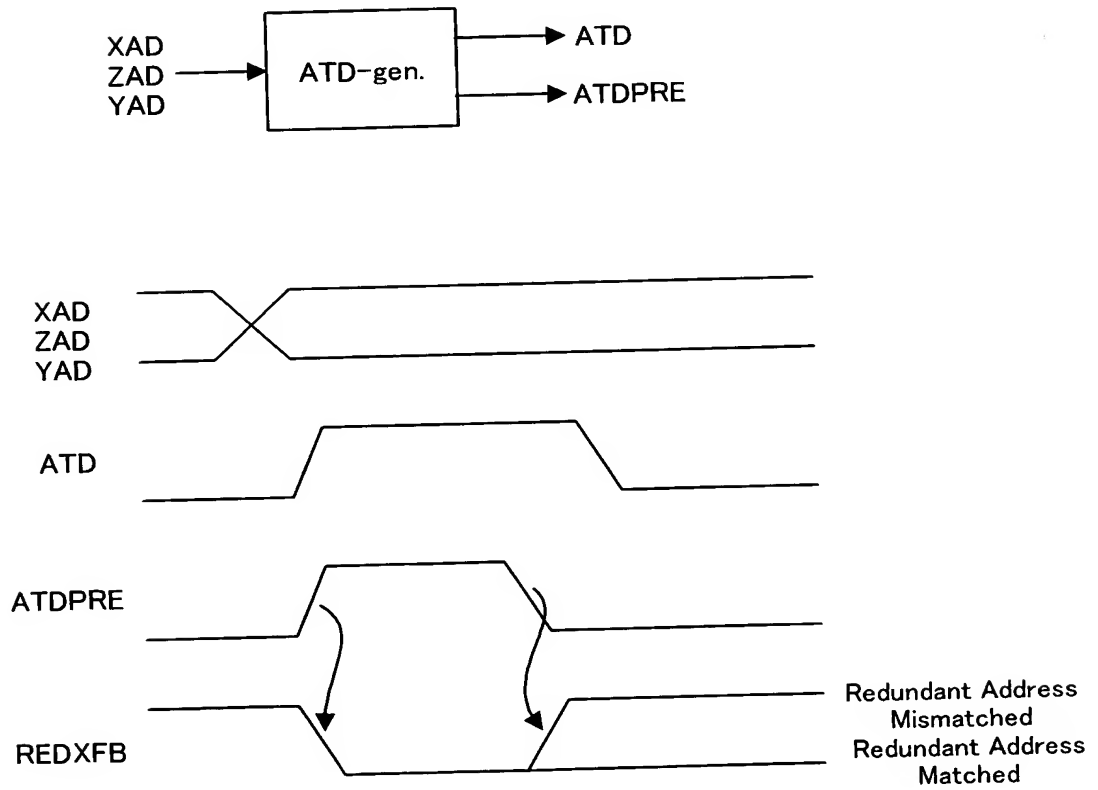


FIG. 9

Redundancy Judgment Circuit

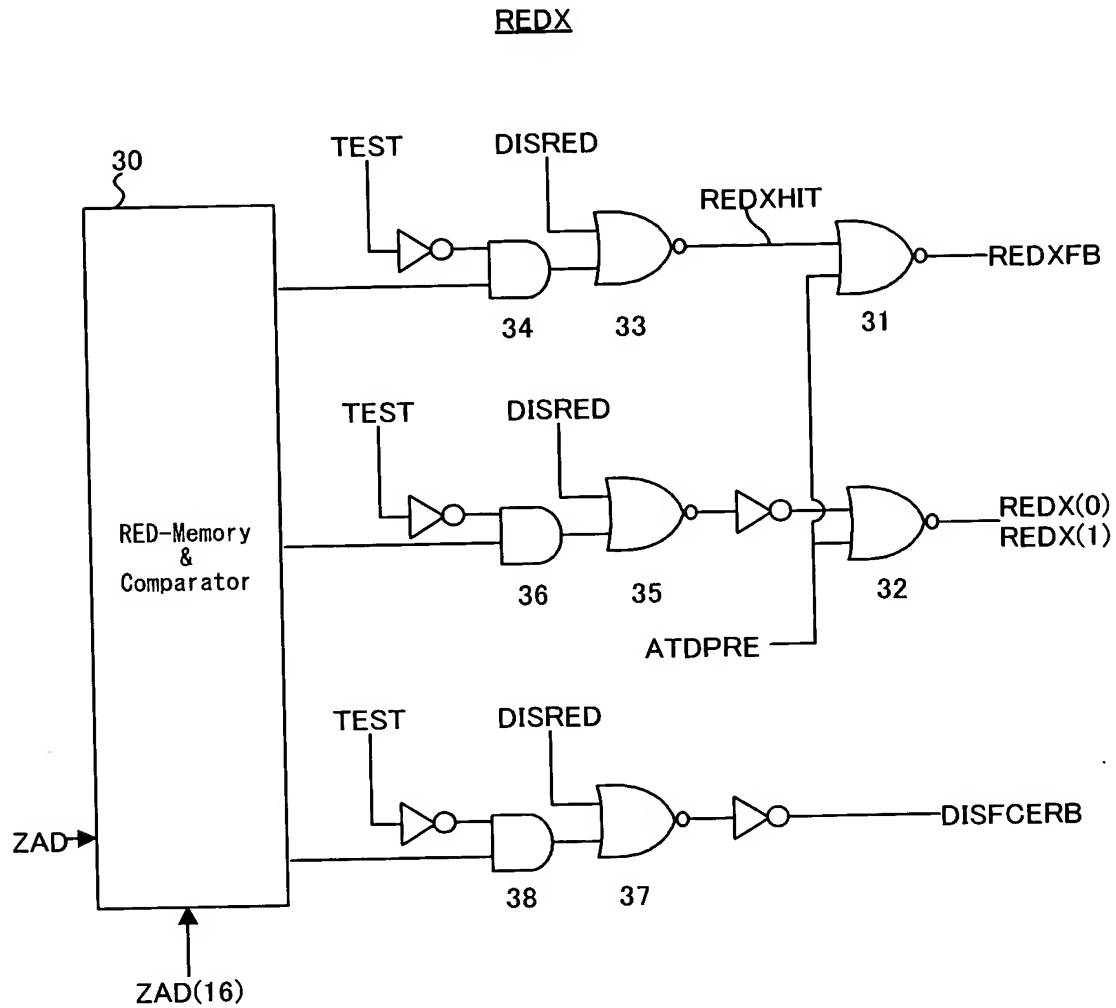


FIG. 10

Local X Decoder

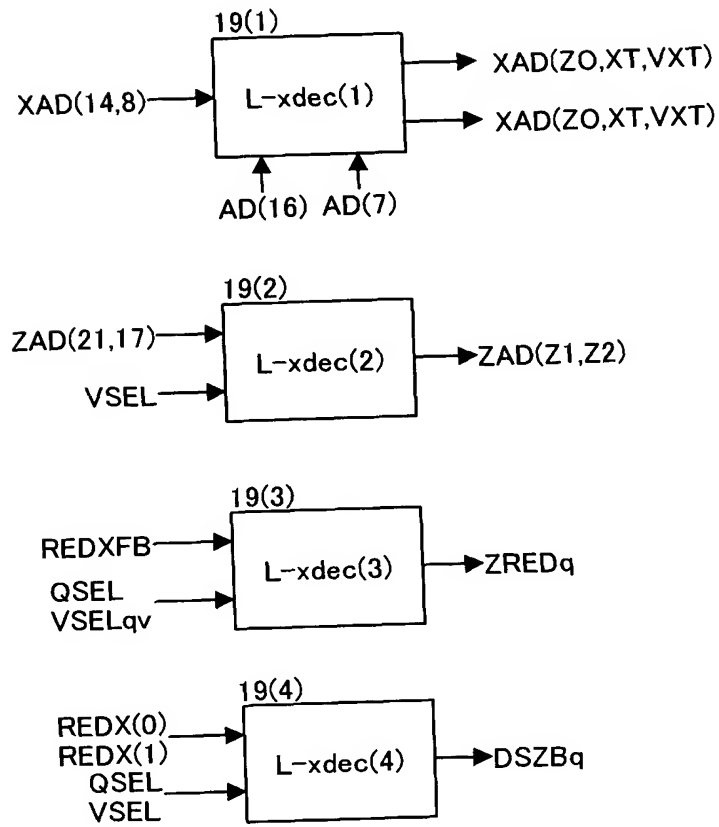


FIG. 11

Boost Power Supply Distribution Circuit

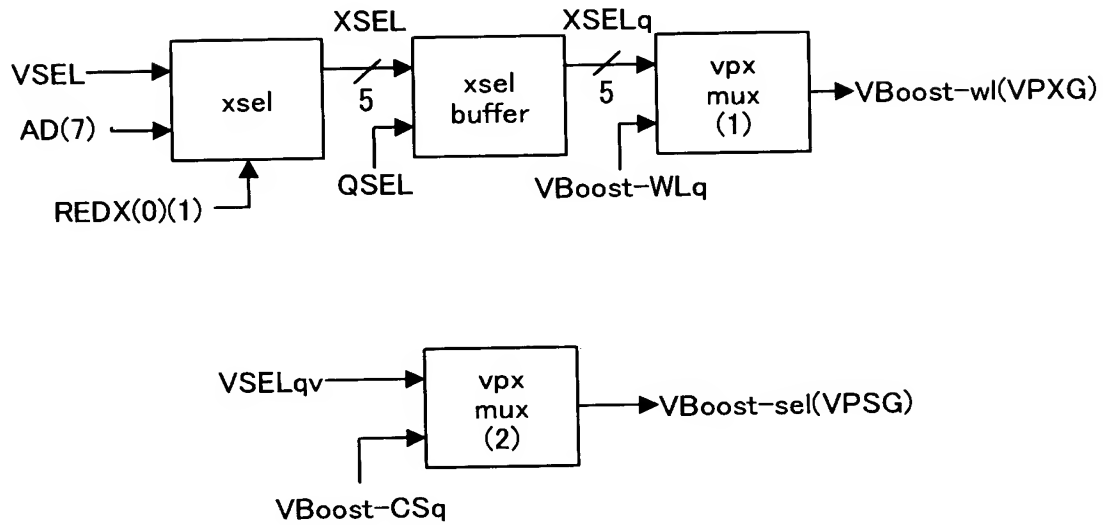


FIG. 12

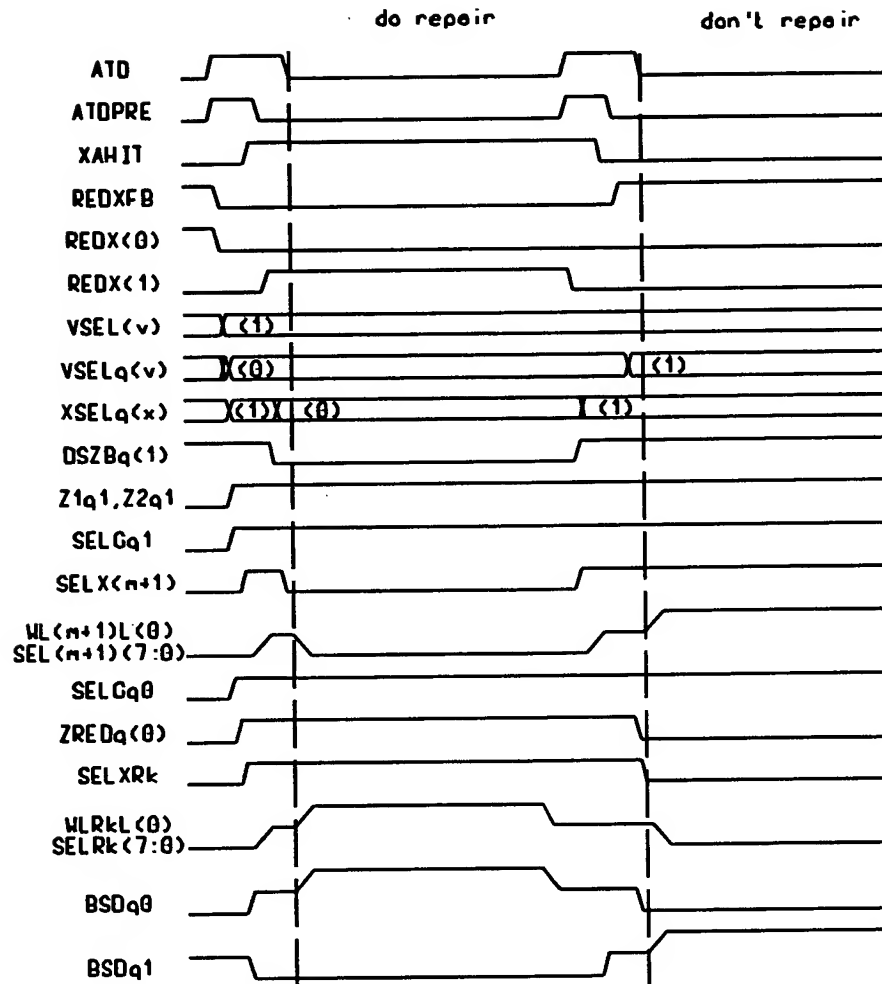


FIG. 13B

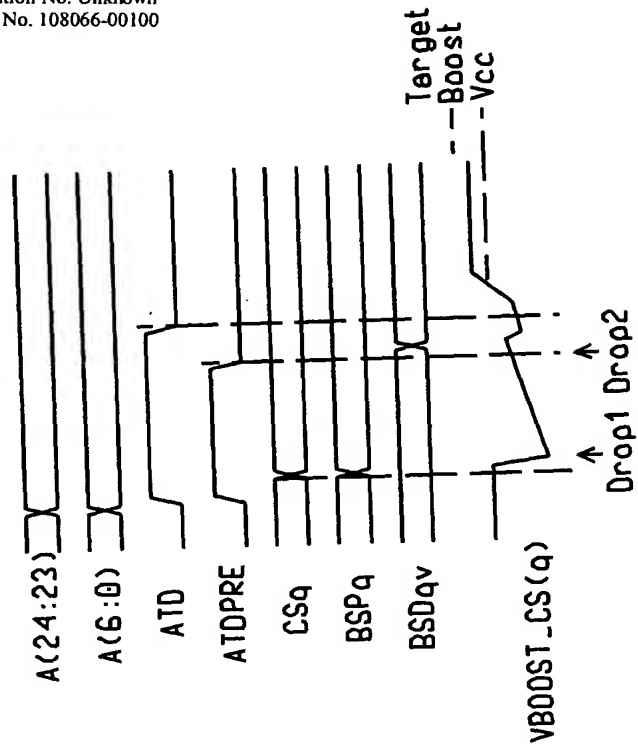


FIG. 13A

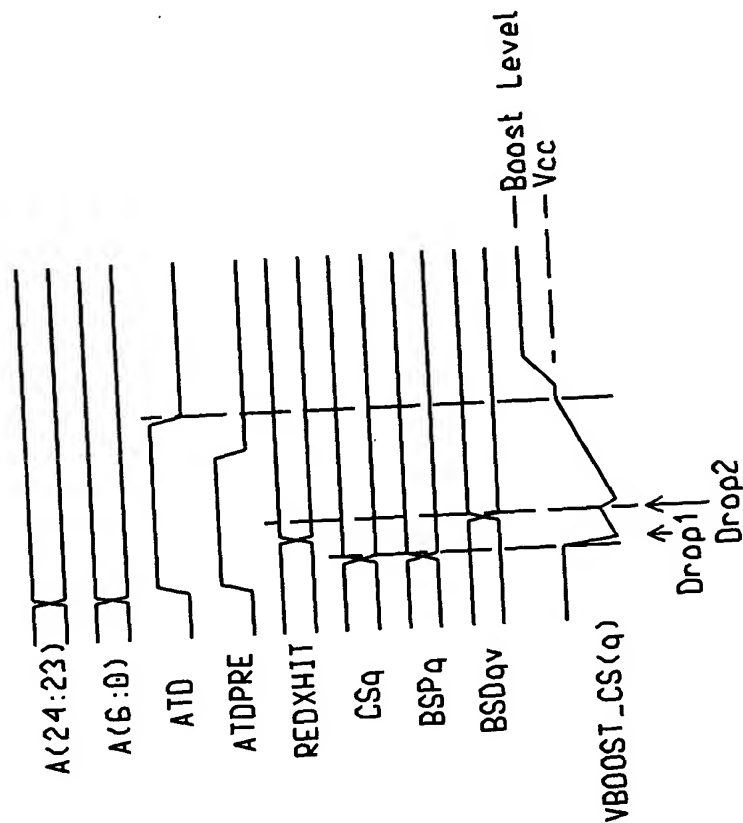


FIG. 14

vsel

